PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-217251

(43)Date of publication of application : 10.08.2001

(51)Int.Cl. H01L 21/322
H01L 21/324
// C30B 29/06

(21)Application number : 2000-331700

(22)Date of filing : 31.10.2000

(71)Applicant : MITSUBISHI MATERIALS SILICON CORP

(72)Inventor : MUROI YUKIO
SHIOTA TAKAAKI
SHIBAZAKI HIDEAKI
KURITA KAZUNARI

(30)Priority

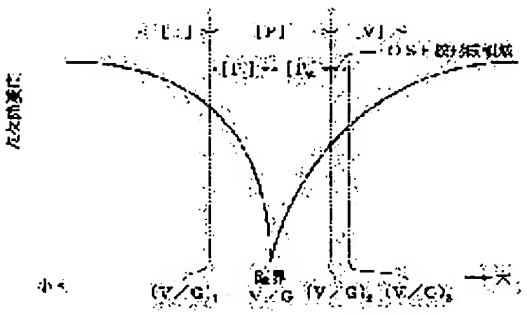
Priority number : 11335327 Priority date : 26.11.1999 Priority country : JP

(54) METHOD OF HEAT-TREATING SILICON WAFER

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a wafer which exhibits an IG effect.

SOLUTION: The region higher than the lowest interstitial silicon concentration capable of forming an interstitial dislocation, which is adjacent to a region [I] where interstitial silicon-type point defects exist dominantly and which belongs to a region [P] where point defect aggregates do not exist, is called [PI]. The region lower than the vacancy concentration capable of forming COP or FPD, which is adjacent to the region [V] where vacant point defects exist dominantly and which belongs to the region [P], is called [PV]. A wafer which is composed of a mixed region of [PV] and [PI], and the hydrogen concentration of which is 0.8×1018 to 1.4×1018 atoms/cm3 (former ASTM) is heated from room temperature to 1,150-1,200°C at the rise rate



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the heat treatment approach of bringing the in thorin chic gettering (following, IG) effectiveness to the silicon wafer with which the floc of the point defect made by the Czochrlski method (henceforth a CZ process) does not exist.
[0002]
[Description of the Prior Art] the minute defect of the oxygen sludge which serves as a nucleus of an oxidation induction stacking fault (it is called OSF Oxidation Induced Stacking Fault and the following.) as a cause of reducing the yield, in the process which manufactures a semiconductor integrated circuit in recent years, and the particle (it is called COP Crystal Originated Particle and the following.) resulting from a crystal -- or existence of an invasion mold rearrangement (it is called LD Interstitial-type Large Dislocation and the following.) is mentioned. The minute defect used as the nucleus is introduced at the time of crystal growth, it actualizes at the thermal oxidation process at the time of manufacturing a semiconductor device etc., and OSF causes a defect, such as an increment in the leakage current of the produced device. Moreover, COP is a pit resulting from the crystal which appears on a wafer front face, when the silicon wafer after mirror polishing is washed with the mixed liquor of ammonia and a hydrogen peroxide. If this wafer is measured with a particle counter, this pit will also be detected as a light-scattering defect with original particle. This COP becomes the cause of degrading electrical characteristics (Time Dependent dielectric Breakdown, TDDB), for example, the dielectric-breakdown property of an oxide film with the passage of time, an oxide-film proof-pressure property (Time Zero Dielectric Breakdown, TZDB), etc. Moreover, if COP exists in a wafer front face, a level difference is produced in the wiring process of a device, and it can become the cause of an open circuit. And also in a component leaver section, it becomes causes, such as leak, and the yield of a product is made low. Furthermore, if LD is also called a rearrangement cluster or the silicon wafer which produced this defect is immersed in the selection etching reagent used as a principal component in fluoric acid, since it will produce a pit, it is also called a rearrangement pit. This LD also becomes the cause of degrading electrical characteristics, for example, a leak property, an isolation property, etc.
[0003] It is necessary to decrease OSF, COP, and LD from the silicon wafer used from the above thing in order to manufacture a semiconductor integrated circuit. The defect-free silicon wafer which does not have this OSF, COP, and LD is indicated by JP,11-1393,A. This defect-free silicon wafer is a silicon wafer cut down from the ingot which consists of a perfect field [P], when the floc of the hole mold point defect within a silicon single crystal ingot and the floc of the silicon mold point defect between grids set to [P] the perfect field which does not exist, respectively. A perfect field [P] intervenes between the field [I] where the silicon mold point defect between grids exists dominantly, and the field [V] where a hole mold point defect exists dominantly within a silicon single crystal ingot. When setting the pull-up rate of an ingot to V (a part for mm/), and setting the temperature gradient of the direction [/ near the interface of silicon melt and an ingot] of an ingot vertical to G (degree C/mm), and thermal oxidation processing is carried out, the value of V/G (a part for 2/[mm] -**) is decided, and the silicon wafer which consists

of this perfect field [P] is made so that OSF generated in the shape of a ring may disappear in a wafer core. On the other hand, there is a manufacturer who asks for the silicon wafer which has the capacity which carries out gettering of the metal contamination which does not have OSF, COP, and LD upwards and is produced at a device process among semiconductor device manufacturers. If it is polluted with a device process by the metal with the wafer which is not fully equipped with gettering capacity, junction leak, the malfunction of the device by the trap level by the metal impurity, etc. will be produced, and, thereby, the yield of a product will fall.

[0004]

[Problem(s) to be Solved by the Invention] However, although the silicon wafer cut down from the ingot which consists of the above-mentioned perfect field [P] does not have OSF, COP, and LD, in heat treatment of a device production process, precipitation of oxygen does not necessarily happen inside a wafer, but it has a possibility that the IG effectiveness may not fully be acquired by this. The purpose of this invention is to offer the heat treatment approach of a silicon wafer of demonstrating the IG effectiveness, even if the oxygen density which consists of a mixing zone of a field [PV] and a field [PI] is the silicon wafer cut down from the ingot of 0.8x1018 - 1.4x1018 atoms/cm3 (old ASTM).

[0005]

[Means for Solving the Problem] Invention concerning claim 1 sets to [I] the field where the silicon mold point defect between grids within a silicon single crystal ingot exists dominantly. When setting to [V] the field where a hole mold point defect exists dominantly and setting to [P] the perfect field where the floc of the silicon mold point defect between grids and the floc of a hole mold point defect do not exist, It is heat treatment of the silicon wafer with which the floc of the point defect started from the ingot which consists of a perfect field [P] does not exist. The characteristic configuration sets to [PI] the field of under the minimum silicon concentration between grids that adjoins the above-mentioned field [I], and belongs to the above-mentioned perfect field [P], and can form an invasion mold rearrangement. When setting to [PV] the field below the hole concentration which adjoins the above-mentioned field [V], and belongs to the above-mentioned perfect field [P], and can form COP or FPD, Consist of a mixing zone of the above-mentioned field [PV] and a field [PI], and the silicon single crystal ingot whose oxygen densities are 0.8x1018 - 1.4x1018 atoms/cm3 (old ASTM) is pulled up. It is in heating the silicon wafer cut down from this ingot with the programming rate of 10-150 degrees C/second from a room temperature to 1150-1200 degrees C under nitrogen, an argon, hydrogen, oxygen, or these mixed-gas ambient atmospheres, and holding for 0 - 30 seconds at 1150-1200 degrees C.

[0006] In invention concerning claim 1, it is the case where the oxygen densities of an ingot are 0.8x1018 - 1.4x1018 atoms/cm3 (old ASTM). When a silicon wafer consists of a mixing zone of a field [PV] and a field [PI] If the silicon wafer cut down from this ingot is heat-treated on the above-mentioned conditions, a precipitation-of-oxygen nucleus will be discovered to the field [PI] to which a precipitation-of-oxygen nucleus is not introduced at the time of crystal growth, and the consistency of that precipitation-of-oxygen nucleus will increase in the field [PV] in which the precipitation-of-oxygen nucleus is introduced into coincidence at the time of crystal growth. Therefore, when the 2nd-step heat treatment and the 3rd-step heat treatment which mention later the wafer which performed the above-mentioned heat treatment are performed, the above-mentioned precipitation-of-oxygen nucleus grows up to be an oxygen sludge (for it to be called BMD Bulk Micro Defect and the following.), and even if it is the wafer which consists of a mixing zone of a field [PV] and a field [PI], it comes to have the IG effectiveness all over a wafer.

[0007] Invention concerning claim 2 the silicon wafer indicated by claim 1 Nitrogen, After performing the 1st-step heat treatment which heats with the programming rate of 10-150 degrees C/second from a room temperature to 1150-1200 degrees C under an argon, hydrogen, oxygen, or these mixed-gas ambient atmospheres, and is held for 0 - 30 seconds at 1150-1200 degrees C It is the heat treatment approach of the silicon wafer characterized by performing the 2nd-step heat treatment which holds a silicon wafer at 700-800 degrees C under nitrogen-gas-atmosphere mind for 4 to 5 hours, and performing further the 3rd-step heat treatment held at 1000 degrees C under an oxygen ambient atmosphere for 16 hours. In invention concerning claim 2, a precipitation-of-oxygen nucleus grows up

to be BMD by performing the 2nd-step heat treatment for the wafer which was mentioned above and which was heat-treated the 1st step, and performing the 3rd-step heat treatment further, and even if it is the wafer which consists of a mixing zone of a field [PV] and a field [PI], it becomes the wafer which has the IG effectiveness on the whole surface.

[0008]

[Embodiment of the Invention] After pulling up an ingot from the silicon melt in a hot zone furnace by the CZ process by the predetermined pull-up rate profile based on Voronkov's (Voronkov) theory, the silicon wafer of this invention slices this ingot, and is produced. Generally, when the ingot of a silicon single crystal is pulled up from the silicon melt in a hot zone furnace by the CZ process, the floc (agglomerates: three-dimensions defect) of a point defect (point defect) and a point defect occurs as a defect in a silicon single crystal. A point defect has two general gestalten of a hole mold point defect and the silicon mold point defect between grids. A hole mold point defect secedes from one of the normal- [one silicon atom / in a silicon crystal lattice] locations. Such a hole becomes a hole mold point defect. On the other hand, if an atom is discovered in locations other than the lattice point of a silicon crystal (interstitial site), this will become a silicon point defect between grids.

[0009] Generally a point defect is formed in the contact surface between silicon melt (melting silicon) and an ingot (solid silicon). However, it is begun by pulling up an ingot continuously to cool the part which was the contact surface with a pull-up. During cooling, a hole mold point defect or the silicon mold point defect between grids joins mutually by diffusion, and the floc (vacancy agglomerates) of a hole mold point defect or the floc (interstitial agglomerates) of the silicon mold point defect between grids is formed. In other words, floc is the three-dimensional structure which originates in the union of a point defect and is generated. The floc of the silicon mold point defect between grids includes the defect called LD mentioned above including the defect to which the floc of a hole mold point defect is called LSTD (Laser ScatteringTomograph Defects) or FPD (Flow Pattern Defects) other than COP mentioned above. In FPD, it is the source of the trace which presents the unique flow pattern which appears when SEKOETCHINGU during 30 minutes of the silicon wafer which sliced the ingot and was produced (Secco etching, etching by the mixed liquor of HF:K2Cr2O7(0.15 mol/l) =2:1) is carried out, and when LSTD irradiates infrared radiation in a silicon single crystal, silicon is a source which has a different refractive index and generates the scattered light.

[0010] When setting the temperature gradient in V (a part for mm/), an ingot, and the ingot near the interface of silicon melt to G (degree C/mm) for the pull-up rate of an ingot, Voronkov's theory is controlling V/G (a part for 2/[mm] -**), in order to grow up a high grade ingot with few defects. This theory explains that express the relation between V/G and point defect concentration in graph, and the boundary of a hole field and the silicon field between grids is determined by V/G for a shaft identically [V/G / concentration / hole mold point defect concentration and / between grids / silicon mold point defect] up for a horizontal axis, as shown in drawing 1 . In more detail, while an ingot with superior hole mold point defect concentration is formed for a V/G ratio above the critical point, an ingot with the superior silicon mold point defect concentration between grids is formed for a V/G ratio below in the critical point. In drawing 1 , the silicon mold point defect between grids of [I] is dominant. The field (V/G) (1 or less) where the silicon mold point defect between grids exists is shown. The field (V/G) (2 or more) where the hole mold point defect of [V] within an ingot is dominant, and the floc of a hole mold point defect exists is shown. [P] shows the perfect field (V/G) (1-(V/G) 2) where the floc of a hole mold point defect and the floc of the silicon mold point defect between grids do not exist. The field [OSF] (V/G) (2-(V/G) 3) which forms an OSF nucleus exists in the field [V] contiguous to a field [P].

[0011] This perfect field [P] is further classified into a field [PI] and a field [PV]. As for [PI], a V/G ratio is a field from the above (V/G) 1 to the critical point, and the V/G ratio of [PV] is a field from the critical point to the above (V/G) 2. That is, [PI] is a field which has the silicon mold point defect concentration between grids of under the minimum silicon mold point defect concentration between grids that adjoins a field [I] and can form an invasion mold rearrangement, and is a field which has the hole mold point defect concentration of under the minimum hole mold point defect concentration that [PV] adjoins a field [V] and can form OSF. When an ingot can pull up the predetermined pull-up rate

profile of this invention from the silicon melt in a hot zone furnace, It is more than the 1st critical ratio (v/G) (1) to which the ratio (V/G) of a pull-up rate to a temperature gradient prevents generating of the floc of the silicon mold point defect between grids. It is decided that it is maintained below at the 2nd critical ratio (V/G) (2) which restricts the floc of a hole mold point defect in the field where the hole mold point defect which exists in the center of an ingot exists dominantly.

[0012] The profile of this pull-up rate is slicing a criteria ingot to shaft orientations experimentally, or is combining these techniques, and is determined by simulation based on above-mentioned Voronkov's theory. That is, after simulation, this decision slices the ingot sliced by shaft orientations in the crossing direction, checks it in the state of a wafer, and is made by repeating simulation further. Two or more kinds of pull-up rates are decided in the predetermined range for simulation, and two or more criteria ingots grow. As shown in drawing 2 , the pull-up rate profile for simulation is adjusted to low 0.5mm pull-up rate for /(c), and an again high pull-up rate (d) from a high 1.2mm pull-up rate (a) like [for /]. the above -- a low pull-up rate may be less than [0.4mm a part for /and it], and its linearity-thing is [the change by the pull-up rate (b) and (d)] desirable. Two or more criteria ingots which were able to be pulled up at a different rate are sliced by shaft orientations at each **. Optimal V/G is determined from the slice of shaft orientations, the check of a wafer, and the correlation as a result of simulation, the optimal pull-up rate profile is continuously determined, and an ingot is manufactured by the profile. An actual pull-up rate profile is dependent on many variables which are not limited to the ability of the diameter of a desired ingot, the specific hot zone furnace used, the quality of silicon melt, etc. to be included.

[0013] When the sectional view of the ingot when reducing a pull-up rate gradually and reducing V/G continuously is drawn, the fact shown in drawing 3 is known. The perfect field where the floc of [I] and a hole mold point defect and the floc of the silicon mold point defect between grids do not exist [the field where the silicon mold point defect between [V] grids exists / the field where the hole mold point defect within an ingot exists dominantly / in drawing 3 dominantly] is shown as [P], respectively. As mentioned above, a perfect field [P] is further classified into a field [PI] and a field [PV]. A field [PV] is a field where the hole mold point defect which does not become floc in a perfect field [P] exists, and a field [PI] is a field where the silicon mold point defect between grids which does not become floc in a perfect field [P] exists. As shown in drawing 3 , the shaft-orientations location P1 of an ingot includes the field where a hole mold point defect exists in the center dominantly. A location P3 includes the ring field where the silicon mold point defect between grids exists dominantly, and a central perfect field. Moreover, since there is also no floc of a hole mold point defect in the center relevant to this invention and there is also no floc of the silicon mold point defect between grids in a part for a edge, a location P2 is a perfect field altogether.

[0014] The wafer W1 corresponding to a location P1 includes the field where a hole mold point defect exists in the center dominantly so that clearly from drawing 3 . Wafer W3 corresponding to a location P3 includes the perfect field of the ring with which the silicon mold point defect between grids exists dominantly, and a center. Moreover, the wafer W2 corresponding to a location P2 is a wafer concerning this invention, since the floc of a hole mold point defect does not have the floc of the silicon mold point defect between grids in the center in a part for a edge, either, it is a perfect field altogether, and it is a field where a field [PV] and a field [PI] are intermingled. Few fields (2 (V/G)-(V/G) 3 of drawing 1) adjacent to the perfect field of the field where this hole mold point defect exists dominantly are fields which have generated neither COP nor LD in a wafer side. However, OSF will be produced, if it heat-treats for 2 to 5 hours at the bottom of an oxygen ambient atmosphere, and 1000-degree-C temperature of **30 degrees C which followed the conventional OSF actualization heat treatment to this silicon wafer W1 and heat-treats at 1130-degree-C temperature of **30 degrees C succeedingly for 1 to 16 hours. As shown in drawing 4 A, with a wafer W1, an OSF ring is generated near [1/2] the radius of a wafer. As for the field where the hole mold point defect surrounded in this OSF ring exists dominantly, COP tends to appear.

[0015] In addition, the floc of point defects, such as COP and LD, may show the value from which detection sensitivity and a minimum-limit-of-detection value differ by the detection approach. In this

specification therefore, the semantics of "the floc of a point defect does not exist" After giving non-stirred SEKOETCHINGU, the silicon single crystal by which mirror plane processing was carried out with an optical microscope When the product of observation area and an etching machining allowance is observed as inspection volume When each floc of a flow pattern (hole mold defect) and a rearrangement cluster (silicon mold point defect between grids) makes the case where an one-piece defect is detected to the inspection volume of 1x10 to 3 cm3 a detection lower limit (1x103 piece/cm3), It says that the number of the flocs of a point defect is below the above-mentioned minimum-limit-of-detection value.
[0016] The silicon wafer of this invention is the wafer W2 mentioned above, and the top view is shown in drawing 4 B. A wafer W2 requires that that oxygen density should be 0.8x1018 - 1.4x1018 atoms/cm3 (old ASTM) in order to make this wafer W2 generate the precipitation-of-oxygen nucleus more than a desired consistency by heat treatment of this invention.
[0017] Next, heat treatment of the above-mentioned silicon wafer W2 is explained. This heat treatment performs the 1st-step heat treatment which heats a wafer W2 with the programming rate of 10-150 degrees C/second from a room temperature to 1150-1200 degrees C under nitrogen, an argon, hydrogen, oxygen, or these mixed-gas ambient atmospheres, and is first held for 0 - 30 seconds at 1150-1200 degrees C. In for 0 second, the holding time means not holding by performing only a temperature up here. Heating introduces a wafer into the interior of the heat treating furnace maintained by the room temperature or the heat treating furnace which is hundreds of times by remaining heat in the case of continuous running, and carries out a temperature up to 1150-1200 degrees C at 50-100 degrees C/second in rate preferably a second 10-150 degrees C /. A programming rate is inferior to a throughput, although a precipitation-of-oxygen nucleus increases in a second in less than 10 degrees C /, and it is not practical. Moreover, at less than 1150 degrees C, when a precipitation-of-oxygen nucleus does not fully increase but the 2nd-step heat treatment and the 3rd-step heat treatment which are mentioned later are performed, a BMD consistency required to do the IG effectiveness so is not obtained. When retention temperature exceeds 1200 degrees C or the holding time exceeds 30 seconds, a slip is generated or the fault to which the productivity of heat treatment falls is produced. Moreover, if a programming rate exceeds a second in 150 degrees C /, the fault which a slip generates by the variation in distribution whenever [self-weight stress or field internal temperature] will be produced. Furthermore, by performing the 1st-step above-mentioned heat treatment, the oxygen donor killer processing of the wafer processes becomes unnecessary.
[0018] Next, the 2nd-step heat treatment which holds a wafer W2 at 700-800 degrees C under nitrogen-gas-atmosphere mind for 4 to 5 hours is performed after the 1st-step heat treatment, and finally, after performing the 2nd-step heat treatment, the 3rd-step heat treatment held at 1000 degrees C for 16 hours is performed under an oxygen ambient atmosphere. In order that a precipitation-of-oxygen nucleus may grow up to be BMD by performing this 2nd-step heat treatment and the 3rd-step heat treatment, the wafer which demonstrates the IG effectiveness is obtained.
[0019]
[Example] Next, the example of this invention is explained with the example of a comparison.
The silicon ingot of p mold with which boron (B) with a diameter of 8 inches was doped using <example 1> silicon single crystal pull-up equipment was pulled up. For 1200mm and crystal orientation, (100) and resistivity were [the die length of the body section / about 10-ohmcm and the oxygen density of this ingot] 1.0x1018 atoms/cm3 (old ASTM). Two ingots were raised on the same conditions, decreasing V/G at the time of a pull-up continuously to -** by 0.18mm2/from -** by 0.24mm2/. One of ingots of it cut the ingot core in the pull-up direction, as shown in drawing 3 , and they investigated the location of each field, cut down the silicon wafer W2 of the location corresponding to P2 of drawing 3 from one [another], and made it the sample. The wafer which serves as a sample in this example is the wafer W2 shown in drawing 4 B which has a field [PV] in a core, has a field [PI] to that perimeter, and has a field [PV] to that perimeter further.
[0020] This wafer W2 that cut down and carried out mirror polishing from the ingot was heated with the programming rate of about 50 degrees C/second from a room temperature to 1150 degrees C under nitrogen-gas-atmosphere mind, and the 1st-step heat treatment was performed, without holding at 1150

degrees C.
[0021] The 1st-step heat treatment was performed at 1150 degrees C like the example 1 except having made into 5 seconds the holding time at the time of heat treatment of a wafer W2 which started and carried out mirror polishing from the same ingot as the <example 2> example 1.
The 1st-step heat treatment was performed at 1150 degrees C like the example 1 except having made into 30 seconds the holding time at the time of heat treatment of a wafer W2 which started and carried out mirror polishing from the same ingot as the <example 3> example 1.
[0022] Except having made into 1200 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 4> example 1, the 1st-step heat treatment was performed like the example 1, without holding at 1200 degrees C.
The 1st-step heat treatment was performed like the example 1 except having made into 1200 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 5> example 1, and having made the holding time into 5 seconds.
The 1st-step heat treatment was performed like the example 1 except having made into 1200 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 6> example 1, and having made the holding time into 30 seconds.
[0023] The 1st-step heat treatment of a wafer W2 which started and carried out mirror polishing from the same ingot as the <example 1 of comparison> example 1 was not performed.
The 1st-step heat treatment was performed like the example 1 except having made into 1100 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 2 of comparison> example 1, and having made the holding time into 5 seconds.
The 1st-step heat treatment was performed like the example 1 except having made into 1100 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 3 of comparison> example 1, and having made the holding time into 30 seconds.
The 1st-step heat treatment was performed like the example 1 except having made into 1100 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 4 of comparison> example 1, and having made the holding time into 60 seconds.
[0024] The 1st-step heat treatment was performed at 1150 degrees C like the example 1 except having made into 60 seconds the holding time of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 5 of comparison> example 1.
The 1st-step heat treatment was performed like the example 1 except having made into 1200 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 6 of comparison> example 1, and having made the holding time into 60 seconds.
The 1st-step heat treatment was performed like the example 1 except having made into 1250 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 7 of comparison> example 1, and having made the holding time into 5 seconds.
The 1st-step heat treatment was performed like the example 1 except having made into 1250 degrees C heat treatment temperature of the wafer W2 which cut down and carried out mirror polishing from the same ingot as the <example 8 of comparison> example 1, and having made the holding time into 30 seconds.
[0025] After holding at 800 degrees C under nitrogen-gas-atmosphere mind for 4 hours by considering the wafer of the <comparative-evaluation> examples 1-6 and the examples 1-8 of a comparison as the 2nd-step heat treatment, respectively, heat treatment held at 1000 degrees C for 16 hours was further performed under the oxygen ambient atmosphere as the 3rd-step heat treatment. After heat-treating, cleavage of each wafer was carried out and the BMD consistency of the part which performs selective etching with a light (Wright) etching reagent, and is equivalent to the field [PV] and field [PI] in a depth

of 350 micrometers from a wafer front face in a wafer front face with observation of an optical microscope, and the existence of a slip were measured further. These results are shown in Table 1.
[0026]
[Table 1]

	熱処理条件		BMD密度(個/cm³)		スリップの有無
	温度(℃)	時間(秒)	領域[Pv]	領域[Pi]	
実施例 1	1150	0	1.8 ×10⁸	1.75×10⁸	無
〃 2	1150	5	1.2 ×10⁸	1.15×10⁸	無
〃 3	1150	30	0.6 ×10⁸	0.5 ×10⁸	無
〃 4	1200	0	2.66×10¹⁰	2.06×10¹⁰	無
〃 5	1200	5	2.06×10¹⁰	1.78×10¹⁰	無
〃 6	1200	30	1.89×10⁹	3.87×10⁹	無
比較例 1	未処理		2.0 ×10⁹	0.5 ×10⁷	無
比較例 2	1100	5	0.5 ×10⁷	0.5 ×10⁷	無
〃 3	1100	30	1.1 ×10⁸	0.5 ×10⁷	無
〃 4	1100	60	1.1 ×10⁸	0.5 ×10⁷	無
〃 5	1150	60	2.5 ×10⁷	0.5 ×10⁷	有
〃 6	1200	60	6.25×10⁹	2.5 ×10⁷	有
〃 7	1250	5	3.68×10⁹	3.43×10⁹	有
〃 8	1250	30	3.27×10⁹	2.94×10⁹	有

[0027] In the part equivalent to the field [PI] of the wafer of the examples 1-6 of a comparison, the BMD consistency did not turn into a BMD consistency (3 or more [Three or more / 5.0x107 //cm / preferably / 1.0x108 //cm]) it is supposed that the IG effectiveness shows up so that clearly from Table 1. Moreover, the slip was generated although the BMD consistency of the part which is equivalent to a field [PV] and a field [PI] about the examples 7 and 8 of a comparison was over 1.0x108 3 [/] cm. In addition, also in the wafer of the examples 5 and 6 of a comparison, the slip appeared. On the other hand, with the wafer of examples 1, 2, 4-6, the BMD consistency of the part equivalent to a field [PV] and a field [PI] exceeded 1.0x108 3 [/] cm, and the slip was not generated. The especially higher BMD consistency with the wafer of examples 4-6 was obtained. In addition, although the BMD consistency was lower than 3 cm 1.0x108 pieces /with the wafer of an example 3, the deposit distribution within a wafer side was uniform.
[0028] The wafer front face was compulsorily polluted with Fe by preparing the wafer W2 of the <example 7> example 1, and dropping and carrying out the spin coat of the solution with which concentration contains Fe of 8x1012 atoms/cm3 to the front face of this wafer W2.
After preparing the wafer W2 which polluted compulsorily the wafer front face of the <example 8> example 7 with Fe and heat-treating this wafer W2 at 800 degrees C for 4 hours, it heat-treated at 1000 degrees C for 16 hours, and Fe element was diffused in the bulk of a wafer.
[0029] The wafer W2 of the example 1 of the <example 9 of comparison> comparison was prepared, and the wafer front face was compulsorily polluted with Fe like the example 7.
the wafer W2 of the <comparative-evaluation 2> examples 7 and 8 and the example 9 of a comparison -- DLTS (Deep Level TransientSpectrosco py) -- Fe concentration on the front face of a wafer was measured by law. The direction distribution map of the diameter of a wafer of Fe concentration of examples 7 and 8 and the example 9 of a comparison is shown in drawing 5 . Fe of 8x1012 atoms/cm3 which is the concentration polluted with the example 9 of a comparison was detected so that more clearly than drawing 5 . On the other hand, in the example 7, Fe concentration was falling in the direction of a path to 2x1012 atoms/cm3 mostly at homogeneity. Moreover, in the example 8, Fe concentration is falling in the direction of a path to 1x1012 atoms/cm3 mostly at homogeneity, and it turns out that the IG effectiveness demonstrates.
[0030]

[Effect of the Invention] As stated above, according to the heat treatment approach of this invention, it consists of a mixing zone of a field [PV] and a field [PI], and the silicon wafer whose oxygen densities are 0.8x1018 - 1.4x1018 atoms/cm3 (old ASTM) is considered as the 1st-step heat treatment. Nitrogen, an argon, hydrogen, By heating with the programming rate of 10-150 degrees C/second from a room temperature to 1150-1200 degrees C under oxygen or these mixed-gas ambient atmospheres, and holding for 0 - 30 seconds at 1150-1200 degrees C In addition to the floc of a point defect not existing, the precipitation-of-oxygen nucleus more than a desired consistency is formed in a field [PI]. Moreover, there is also an advantage from which the oxygen donor killer processing currently performed conventionally becomes unnecessary. Then, since the precipitation-of-oxygen nucleus formed in the 1st-step heat treatment by holding a silicon wafer at 700-800 degrees C under nitrogen-gas-atmosphere mind as the 2nd-step heat treatment for 4 to 5 hours, and holding at 1000 degrees C under an oxygen ambient atmosphere as the 3rd-step heat treatment further for 16 hours grows up to be an oxygen sludge, the IG effectiveness can be demonstrated all over a wafer.

[Translation done.]